AMENDMENTS TO THE CLAIMS

Please cancel claims 2, 5 and 6 without prejudice. Please add claims 30-32.

1. (CURRENTLY AMENDED) A method for verifying connectivity of one or more analog signals through an analog design ~~verification~~, comprising the steps of:

(A) creating a Hardware Description Language model of said analog design;

~~(A)~~ (B) generating said one or more analog signals utilized by said ~~an~~ analog design;

(C) creating a unique digital signature for each of said one or more analog signals and adding code to cause each of said unique digital signatures to be generated within a digital simulator;

~~(B)~~ (D) generating one or more source signals by adding ~~a~~ each of said unique digital ~~signature~~ signatures to each of said analog signals; ~~and~~

~~(C)~~ (E) modeling said analog design using said source signals in place of said analog signals in said model; and

(F) ~~for~~ verifying said connectivity using said digital simulator to perform one or more simulations of said analog design with said source signals propagating through said analog design.

2. (CANCELED)

3. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures corresponds to a type of said analog signals having a predetermined parameter.

4. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures comprises a unique pulse width.

5. (CANCELED)

6. (CANCELED)

7. (CURRENTLY AMENDED) The method according to claim ~~2~~ 1, wherein verifying said connectivity ~~performing said simulations further~~ comprises the sub-step of:

verifying ~~a~~ said model of said analog design for an analog block within said analog design configured to receive at least a particular one of said analog signals.

8. (CURRENTLY AMENDED) The method according to claim 7, wherein verifying said model ~~further~~ comprises the sub-step of:

verifying an output signal of said analog block for said unique digital signature associated with said particular one of said analog signals.

9. (CURRENTLY AMENDED) A method for testing a Hardware Description Language model of an analog design ~~device~~, comprising the steps of:

(A) generating one or more attributed signals each (i) having a unique digital signature to be generated within a digital simulator by adding code to a source block within said model of said analog design and (ii) presented by ~~a~~ said source block; ~~within said model of said analog device; and~~

(B) using said digital simulator to perform one or more simulations of said model of said analog design; and

~~(B)~~ (C) verifying connectivity of said attributed signals to a destination block within said model of said analog design ~~device~~ by verifying reception of said unique digital signatures associated with each of said attributed signals at said destination block.

10. (CURRENTLY AMENDED) The method according to claim 9, further comprising the step of:

disabling processing of a particular one of said attributed signals if said particular attributed signal is not verified at said destination block.

11. (CURRENTLY AMENDED) The method according to claim 9, further comprising the step of:

verifying ~~a~~ said model of said analog design for said destination block configured to receive at least one of said attributed signals.

12. (CANCELED)

13. (CANCELED)

14. (CANCELED)

15. (CANCELED)

16. (CANCELED)

17. (CANCELED)

18. (CANCELED)

19. (CANCELED)

20. (CANCELED)

21. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures comprises a plurality of pulses.

22. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures comprises a varying frequency signal.

23. (CURRENTLY AMENDED) A system comprising:

a model of an analog design including a Hardware Description Language modeled ~~a~~ source for creating (i) a plurality of analog signals utilized by said analog design, (ii) a plurality of unique digital signatures and (iii) one or more source signals by adding each of said unique digital signatures to each of said analog signals~~, at least one of said signals representing an analog signal having a digital signature~~; and

a digital simulator ~~connected to said source and~~ configured to (i) simulate a Hardware Description Language model created for said ~~an~~ analog design, (ii) receive said source signals~~, and~~ (iii) incorporate code to generate said unique digital signatures within said digital simulator and (iv) verify a connectivity of said analog signals through said analog design by performing one or more simulations of said analog design with said source signals propagating through said analog design ~~signal in said analog design using said digital signature~~.

24. (CURRENTLY AMENDED) The system according to claim 23, wherein said source comprises an analog source block configured to generate said analog signals ~~signal~~.

25. (CURRENTLY AMENDED) The system according to claim 24, wherein said source further comprises an adder block configured to (i) generate said unique digital signatures ~~signature~~ and (ii) add said unique digital signatures ~~signature~~ to said analog signals ~~signal~~.

26. (CURRENTLY AMENDED) The system according to claim 25, wherein said source further comprises a digital source block configured to generate at least one ~~of said signals representing a~~ digital signal used by said digital simulator.

27. (CURRENTLY AMENDED) The system according to claim 23, wherein each of said digital signatures comprise ~~signature comprises~~ a plurality of pulses.

28. (CURRENTLY AMENDED) The system according to claim 27, wherein each of said pulses have a unique width to identify said analog signals ~~signal~~.

29. (CURRENTLY AMENDED) The system according to claim 27, wherein each of said digital signatures ~~signature~~ has a varying frequency.

30. (NEW) The method according to claim 1, wherein said Hardware Description Language model comprises a Verilog model.

31. (NEW) The method according to claim 9, wherein said Hardware Description Language model comprises a Verilog model.

32. (NEW) The system according to claim 23, wherein said Hardware Description Language model comprises a Verilog model.